JOINT SESSION 2: Foundry Functional Diversification- Design Perspectives (All Invited Talks)
Tuesday, April 28, 1:30 P.M. ~ 4:45 P.M.
Ballroom B
Co-chairs: Carlos Mazure, Soitec, France
Jiun-In Guo, National Chiao Tung University, Taiwan

1:30 P.M.
JS21 Specialty Technology for IoT
Gene Li
UMC, Taiwan

This presentation intends to reveal UMC’s viewpoints on how IoT will change the landscape of foundry service. The ever-evolving applications and requirements have substantially impacted chip specs and the supporting foundry technologies and IP’s, accordingly. This talk will elaborate the interlocks from application specs, design needs, and process technologies and IP’s adapting to new power/performance/cost requirements in IoT era. In addition, the fragmented application nature in IoT market requires comprehensive technology portfolio support from foundry house. Extensive new technology platform offerings, optimizing for ultralow power consumption and best C/P value, and services are to be introduced.

2:05 P.M.
JS22 Low-Power IC Design Challenge
Cheng-Chih Mao
MediaTek, Taiwan

Green design becomes more important in these years. How to enhance the power efficiency is the mainstream of the SoC design. This work will talk about the challenges and possible solutions of each stage in the IC design flow, from the architecture level to the production level.

2:40 P.M.
JS23 The Sum of the Parts: Overcoming Leading Edge Design Challenges by Working in Partnership
Tim Whitfield
ARM, Taiwan

Providing IP in today’s fast moving technology industry means much more than just delivering RTL. All of ARM’s partners are under pressure to produce increasingly advanced products to ever demanding consumers, whilst pressures on cost and timescales are also increasing. The complexities of advanced process nodes and increasing functionality compound the problem as our partners try to provide innovative products from tiny sensors to powerful servers.

This presentation will demonstrate how ARM works with its eco-system partners to ensure that the foundations are properly laid to enable the ARM partnership to continue to deliver game changing technology. Collaborating across the industry from silicon process to software, the ARM eco-system works together to deliver all of the building blocks and ensure that the sum of the parts is greater than the whole.

3:15 P.M. Break
During the R&D of advanced nanometer CMOS technologies such as 20nm and beyond, we implemented in-house 3-D capacitance extraction software to provide R&D engineers with an accurate modeling tool to optimize the complex 3-D nanometer dimensions and materials that may be used for competitive CMOS devices in terms of power consumption, performance, and area. Our extractor solves 3-D Laplace's equation and extracts capacitances and resistances targeting accurate on-chip parasitic modeling. In essence, the numerical method we adopted can model flexible grids for arbitrary shapes in nanometer CMOS devices. Robust and rigorous algorithms are described that allow the R&D engineers to monitor the convergence and specify the corresponding accuracy level based on the resource and allowed turnaround time.

Due to various manufacture difficulties in nano-scale semiconductor devices, certain layout patterns cannot be manufactured properly and cause significant yield loss. Due to the time to run through complete lithography simulation, it is impossible to identify all of them before silicon manufacture. Therefore, post-silicon physical failure analysis is needed to find them one-by-one to improve yield iteratively with each re-spin. However, physical failure analysis is time-consuming such that each re-spin can take a long time. To speed-up yield ramp-up, we proposed to automatically identify as many layout patterns as possible by using volume diagnosis from post-silicon manufacture failure data. Typically volume diagnosis uses two procedures. First, responses from failing devices are analyzed using defect diagnosis tools. Next the results of diagnoses are analyzed using statistical, data mining and machine learning techniques to effectively determine the underlying problematic layout patterns. In this presentation, we will discuss the procedures and statistics methods for analyzing diagnosis data and put special attention to the link between defects and layout patterns.